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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/680,878	XUE ET AL.
	Examiner	Art Unit
	Ly D. Pham	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,12-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 16* is/are allowed.

6)☒ Claim(s) *1-7,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed November 09, 2005 has been entered. Claims 1, 12, and 14 have been amended. Claims 8 – 11 and 15 have been canceled.

2. The amendment overcomes the objection of claims 14 and 16 in the Previous Office Action mailed on August 12, 2005.

Specification

3. Claims 1 – 7 and 12 – 13 are objected to because of the following informalities:

Claims 1 – 7 and 12 – 13 are objected to as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1 and 12 fail to correspond in scope with that which applicant(s) regard as the invention can be found in the reply filed in November 09, 2005. In that paper, applicant has stated that "The hot carriers are injected into and stored on at least one charge storage dielectric layer **from a drain side of the memory cell**, ...", and also in claims 1 and 12, "... injection of hot carriers from the drain of the memory cell ... effects programming of the memory cell". This statement indicates that the invention is different from what is defined in the specification. Because without clearly defining in the claims that the hot carriers must be "hot holes", paragraph 0046 has clearly indicated that "The substrate bias contributes to the generation and/or acceleration of hot electrons near the drain junction." Therefore, according also to applicants' disclosure, paragraphs 0040 and

0041, these hot carriers (whether primary or even second-impact) are clearly defined as the hot **electrons**, which are "... attracted towards the gate 5 by the gate voltage and will be **injected near the drain 4 side** of the memory device into the dielectric stack ...". As a result, the description of the programming mechanism, as disclosed in the specification (please read paragraphs 0039 – 0044 very carefully), contradicts to that of what are claimed and remarked—hot carriers from the drain side.

Correction and/or clarification are required in order to overcome this objection. For the purpose of Examination, so long the memory cell structures disclosed in the prior arts, including the applied voltage conditions, qualify those that are required in the claims, they are asserted to be capable of performing the mechanism set forth in the claims (with logical interpretations albeit the issues being addressed above).

Response to Arguments

4. Applicant's arguments filed November 09, 2005 have been fully considered.

Below please find the claims rejection responsive to the remarks, in which applicant indicated that the charge storage layer of dielectric material, nitride to be specific.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 7, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US Pat 6,850,440 B2) in view of Eitan (US Pat 5,768,192).

Regarding **claims 1, 6, 7, and 12**, Lin et al. disclose a method for programming a single bit nonvolatile memory cell comprising a semiconductor substrate (figs. 4, 5, 7, or 8, P-substrate) including a source (fig. 4B, source 122), a drain (fig. 4B, drain 114), and a channel in between the source and the drain; and a control gate that comprises a control gate electrode (fig. 4B, control gate electrode 116) and a dielectric stack (fig. 4B, layer 124 and the top and bottom dielectric layers over above and below layer 124. See also col. 6, lines 38 – 49, col. 8, lines 36 – 47. Dielectric stack being the Oxide-Nitride-Oxide layer), the gate electrode being separated from the channel by the dielectric stack (fig. 4B), the dielectric stack comprising at least one charge storage dielectric layer (fig. 4B, layer 124), wherein the method for programming (col. 3, table 2, under conventional CHISEL programming voltages) comprises:

applying electrical ground to the source (Vsource = 0 Volts);

applying a first voltage having a first polarity to the drain (Vdrain = 1.1 to 3.3 Volts);

applying a second voltage of the first polarity to the control gate (Vcg = 3 to 5 Volts);

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate (Vpwell/psub = -0.5 to –4 Volts),

wherein the first, second, and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers, at least some of the hot carriers being generated by a secondary impact ionization mechanism (see above), and injected and stored on the at least one charge storage dielectric layer (col. 1, line 66 – col. 2, line 4, and lines 52 – 58. See also col. 3, line 15 – col. 4, line 13. By charge trapping layer, the floating gate electrode must be injected with the hot electrons and retains—stores those electrons in order to be programmed! Also, with the given bias conditions, electrons induced from the drain-to-source current that gain sufficient energy, hence hot electrons, will jump or inject into the floating gate and trapped—stored therein. See col. 1, lines 31 – 42, consequently, hot carriers—energetic electrons may be attracted to the gate voltage and jump to the charge trapping layer near the drain side, but definitely not from the drain side. Specification paragraph 0041).

Regarding **claims 2 and 13**, Lin et al. also show the method of claim 1, wherein absolute values of each of the first, second, and third voltages are 5V or less (see table 2, where all applied voltages have absolute values of 5 volts or less).

Regarding **claim 3**, Lin et al. also show the method of claim 1, wherein a difference of absolute values of any two voltages of the first, second, and third voltages is 1.5V or less (see table 2).

Regarding **claim 4**, Lin et al. also show the method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and third voltage is at least 4V (if Vcg is 3V and Vpwell/psub is -1V, the effective Vgate-substrate is 4V).

Regarding **claim 5**, Lin et al. also show the method of claim 4, wherein absolute values of each of the second and third voltages are 5V or less (see above, Vgate-substrate is 4V, which is less than 5V).

Although Lin et al. disclose a method of programming a single bit nonvolatile memory cell as disclosed in claims 1 – 7, 12, and 13, except the dielectric stack being an ONO stack, wherein a nitride layer is the charge trapping layer, this feature has been taught by Eitan (abstract: ONO trapping dielectric). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Eitan to the disclosures by Lin et al., so that programming time is greatly reduced (Eitan: abstract).

7. Claims 1 – 7, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bude et al. (US Pat 5,838,617) in view of Eitan (US Pat 5,768,192).

Regarding **claims 1, 2 and 12**, Bude et al. disclose a method for programming a single bit nonvolatile memory cell comprising a semiconductor substrate (fig. 1, substrate 30) including a source (fig. 1, source 50), a drain (fig. 4B, drain 70), and a channel in between the source and the drain (fig. 1, channel 80); and a control gate that comprises a gate electrode (fig. 1, gate electrode 40) and a dielectric stack (fig. 1, layers 20, 10, and 60), the gate electrode being separated from the channel by the dielectric stack (fig. 1, gate electrode 40 separated from channel 80 by layers 20, 10, and 60), the dielectric stack comprising at least one charge storage dielectric layer (fig. 1, layer 10), wherein the method for programming (col. 3, lines 30 – 67) comprises:

applying a first voltage having a first polarity to the drain (drain-source bias voltage V_{DS} less than about 5 Volts);

applying a second voltage of the first polarity to the control gate (control gate-source bias voltage V_{CS} of about 10 volts or less. See also col. 10, lines 17 – 26);

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate ('negative substrate-source bias voltage V_{BS} of about –0.5 to –4 volts);

applying electrical ground to the source (since all voltages are with respect to the source, inherently, the source acts as reference potential and is virtually at ground),

wherein the first, second, and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers generated by a secondary impact ionization mechanism (see above), the hot carriers being injected into the at least one charge storage dielectric layer (col. 3, lines 31 – 48. Hot carriers are hot electrons, which are injected into the floating gate electrode, where they are stored to effect programming of the cell. See also above).

Regarding **claim 3**, Bude et al. also disclose the method of claim 1, wherein a difference of absolute values of any two voltages of the first, second, and third voltages is 1.5 V or less (within the ranges disclosed, if V_{DS} is 4.5 volts and V_{BS} is –4volts, the difference of absolute values of these two voltates is 0.5 volts, which is 1.5V or less).

Regarding **claim 4**, Bude et al. also disclose the method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and the third voltages is at

least 4 V (again, within the allowable ranges disclosed, if V_{BS} is –3 Volts and V_{CS} is set at 1V, the effective gate-to-substrate voltage is 4V).

Regarding **claim 5**, Bude et al. also disclose the method of claim 4, wherein absolute values of each of the second and third voltages are 5V or less (see above for the exemplary condition where effective gate-to-substrate voltage is 4V, which is 5V or less).

Regarding **claim 6**, Bude et al. further disclose the method of claim 1, wherein the charge storage dielectric layer is positioned between two oxide layers (col. 1, lines 36 – 52, wherein 20 and 60 are the two insulator layers).

Regarding **claim 13**, since Bude et al. have shown all applied bias voltages each having an absolute value of 5V or less, therefore, it is considered inherent that the peripheral circuitry comprises circuitry for generating an on-chip voltage having an absolute value of 5V or less.

Although Bude et al. disclose a method of programming a single bit nonvolatile memory cell as disclosed in claims 1 – 6, 12, and 13, except the dielectric stack being an ONO stack, wherein a nitride layer is the charge trapping layer, as also claimed in **claim 7**, this feature has been taught by Eitan (abstract: ONO trapping dielectric). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Eitan to the disclosures by Bude et al., so that programming time is greatly reduced (Eitan: abstract).

Allowable Subject Matter

8. **Claims 14 and 16** are allowed.

9. The statement for the Reason of Allowance was provided in the previous Office Action, mailing date August 12, 2005.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
November 24, 2005